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09/891,310	06/27/2001	Masahito Suzuki	108066-00037	1647

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EXAMINER	
BRITT, CYNTHIA H	

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2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/891,310	Applicant(s) SUZUKI, MASAHITO	
	Examiner Cynthia Britt	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *4,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings submitted on June 27, 2001 are acceptable.

Specification

The disclosure is objected to because of the following informalities:

There are multiple instances of words being run together (without spaces between the words) which renders the specification unintelligible at various points.

Abstract, lines 5,6, and 11

Page 1, lines 16 and line 17

Page 2, line 5,19, and 21

Page 3, line 23

Page 4, line 14

This problem continues throughout the abstract, specification and claims. Although every instance of this has not been pointed out, Applicant is requested to carefully proofread the entire specification and correct this problem.

Appropriate correction is required.

Claim Objections

Claims 4, 7, and 8 are objected to because of the following informalities:

As indicated above in the objection to the specification, there are multiple instances of words being run together (without spaces between the words) which render the claims unintelligible at various points.

Claim 4, line 2

Claim 7, line 3

Claim 8, line 4

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 5, and 9, the terms "serial parallel" and "serial-parallel" are used. Although the terms "serial parallel" and "serial-parallel" appear to be the same, these terms do not seem to be used interchangeably within the claims. It is therefore unclear to the examiner if there is a different meaning to these separate terms, what that

difference is. Therefore it is requested of the applicant in response to this office action to clarify the meaning or difference in meaning of these terms.

The dependent claims 2-4, 6-8, and 10 inherit the 35 U.S.C. 112, second paragraph issues of the independent claims 1, 5, and 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhong et al. U.S. Patent No. 6,014,763 in view of Whetsel U.S. Patent No. 6,405,335.

As per claims 1,5, and 9, Dhong et al. substantially teach the claimed circuitry for testing in an integrated circuit, using the steps of transmitting a scan input in parallel from a tester to the integrated circuit, converting the scan input at the integrated circuit

from parallel to serial, and passing the serial scan input through scan circuitry of the integrated circuit, to create a serial scan output. The transmitting step includes the steps of transmitting a scan data input in parallel, and transmitting a scan enable input in parallel. If loading the caches through the scan chain is desired, the control signal (cache enable) is also transmitted in parallel. The scan output can further be converted from serial to parallel, and the scan output transmitted in parallel from the integrated circuit to the tester. The transmitting step takes place at a speed of the tester clock signal, but the scan operates at the full operational speed of the device under test. An optional external scan input can be used to run the scan at a lower speed. A bypass mechanism can also be used to skip the actual scan in order to check the scan interface. The scan enable input can be distributed to the scan circuitry using a plurality of multiplexers configured in a tree structure. At-speed scan testing can be achieved for speeds in excess of 1 GHz. (column 3 lines7-33) Not explicitly disclosed is that the inputs are buffered.

However, in an analogous art, Whetsel teaches an integrated circuit for testing in which the input signal is input to a series of input buffers connected to the individual scan paths (column 28, lines 45-61). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the input buffer circuitry connected to the scan paths taught by Dhong et al. This would have been obvious as suggested by Whetsel in order to separate the signals to each path and to reduce the power consumption (column 28, lines 36-44) during a scan sequence.

As per claims 2, 3, 6, 7, and 10, Dhong et al. teach that the scan enable input can be distributed to the scan circuitry using a plurality of multiplexers configured in a tree structure. As further illustrated in FIG. 5, the scan chain is preferably implemented using additional multiplexer input ports to reduce the load on each distributed signal. The scan enable line is fed to multiple inputs of another multiplexer/latch, which splits the signal into different lines that are fed to second-level multiplexer/latches. The outputs of each of the second-level multiplexer/latches can be similarly split to provide another four inputs to four third-level multiplexer/latches. In this manner, 48 identical scan enable outputs can be provided. This tree structure for distributing the scan chain can allow the scan speed to actually exceed the processor's normal operational speed. In a similar manner, another multiplexer/latch can be used as illustrated in FIG. 6, to divide the cache enable signal into two identical signals, one for the instruction cache, and one for the data cache. (Column 5 lines 46-62 and Fig 5 and Fig 6)

As per claims 4, and 8, Whetsel teaches that when the integrated circuit's functional circuitry is configured for testing, all functional registers (flip/flops or latches) in the integrated circuit are converted into scan registers that form the parallel scan paths shown. Also, during test configuration, all combinational logic in the integrated circuit that was associated with the functional registers remains associated with the scan registers after the conversion. This conversion of an integrated circuit's functional circuitry into scan paths and combinational logic is well known. (column 5 lines 40-49)

Conclusion

U.S. Patent No. 4,710,933 Powell et al.

The present invention disclosed and claimed herein comprises a testable logic module. The logic module is comprised of a plurality of defined logic circuits which are operable to function together and provide a predetermined module function. Each of the logic circuits has a plurality of control/observation locations embedded therein for allowing testing thereof. The logic circuits are interfaced with a common internal bus through parallel registers. Each of the parallel registers comprises parallel control/observation locations. During testing, each of the parallel registers is separately addressed and loaded with parallel test vectors and then the embedded control/observation locations are connected in the serial chain for serially shifting test vectors therein. After loading, the test vectors are applied to the associated logic circuit and the results stored in both the parallel registers and the serial control/observation locations. The parallel registers are then unloaded through the common bus by selectively addressing each of the registers and outputting the results onto the bus. The serial control/observation locations are then unloaded through the serial data link to allow observation of these results.

U.S. Patent No. 6,646,460 Whetsel

The integrated circuits include sequential and combinatorial logic used by the integrated circuit during normal functioning thereof. Testing of that logic can occur by sending test vectors in parallel or serial form to input pins of the integrated circuit. The

test results can either be read as a serial data stream or as a parallel-delivered data stream. If the test information and results occur in parallel fashion, than automated test equipment can be used which do not require compliance with having a single serial fed test vector input and test result output, normally found in a TAP application. A parallel/serial multiplexer is used to select whether the integrated circuit receives parallel or serial test vectors, and another parallel/serial multiplexer is used to select whether the test results are to be delivered in parallel or serial fashion. A test access port controller is linked to various boundary scan cells, and control signal generators within the controller orchestrate movement of test data or normal functional data into and from the integrated circuit core logic. Parallel fed test vectors can be shifted from the input cells as serial fed test vectors and then back to the input cells, where the test vectors can then be sent to the core logic among numerous conductors in parallel fashion. Likewise, the test results can be converted from a parallel to serial form and fed back to the output cells, whereupon the test results can be sent to the test equipment as parallel-delivered test results.

U.S. Patent No 6,430,718 Nayak

The integrated circuits include sequential and combinatorial logic used by the integrated circuit during normal functioning thereof. Testing of that logic can occur by sending test vectors in parallel or serial form to input pins of the integrated circuit. The test results can either be read as a serial data stream or as a parallel-delivered data stream. If the test information and results occur in parallel fashion, than automated test

equipment can be used which do not require compliance with having a single serial fed test vector input and test result output, normally found in a TAP application. A parallel/serial multiplexer is used to select whether the integrated circuit receives parallel or serial test vectors, and another parallel/serial multiplexer is used to select whether the test results are to be delivered in parallel or serial fashion. A test access port controller is linked to various boundary scan cells, and control signal generators within the controller orchestrate movement of test data or normal functional data into and from the integrated circuit core logic. Parallel fed test vectors can be shifted from the input cells as serial fed test vectors and then back to the input cells, where the test vectors can then be sent to the core logic among numerous conductors in parallel fashion. Likewise, the test results can be converted from a parallel to serial form and fed back to the output cells, whereupon the test results can be sent to the test equipment as parallel-delivered test results.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

Albert DeCady
Primary Examiner